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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: John W. Rapp, Larry Jackson, Mark Jones, Troy Cherasaro

Title: PROGRAMMABLE CIRCUIT AND RELATED COMPUTING MACHINE AND METHOD

Serial Number: 10/684,057

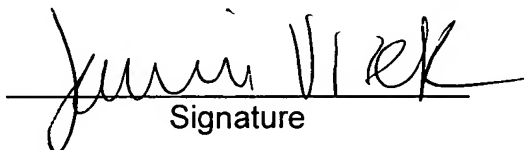
Filing Date: October 9, 2003

Examiner/Unit: Richard B. Franklin/2818

Attorney Docket No.: 1934-14-3

CERTIFICATE OF MAILING OR TRANSMISSION

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A copy of the cited non-U.S. references are enclosed.

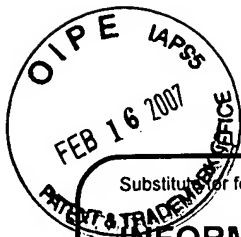
**Certification Under Section 1.97(e)**

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this statement.

Respectfully submitted,

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 1

**Complete if Known**

Application Number	10/684,057
Filing Date	October 9, 2005
First Named Inventor	John Rapp
Art Unit	2181
Examiner Name	Richard B. Franklin
Attorney Docket Number	1934-14-3

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		BAKSHI S; GAJSKI D D; "Partitioning and Pipelining for Performance-Constrained Hardware/Software Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, NR. 4, PG. 419-432, (1999-12-00), XP000869229	

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